physica status solidi a
www.pss-a.com

Reliability Aspects of 28 nm BEOL-Integrated Resistive Switching Random Access Memory

Stefan Wiefels, Nils Kopperberg, Karl Hofmann, Jan Otterstedt, Dirk Wouters, Rainer Waser, and Stephan Menzel*

Approaching the application of redox-based resistive switching random access memory (ReRAM), the research focus shifts more and more toward different aspects of reliability. Herein, it is vital to account for the statistics in large memory blocks, as certain failure mechanisms are observed to only affect a few bits per million. In a cooperation between RWTH Aachen and Infineon Technologies, the variability, retention, and endurance of filamentary valence change memory, integrated into 28 nm CMOS on Mbit scale are comprehensively studied. This article reviews the main findings of this project. It is found that the programmed states follow characteristic normal or log-normal statistics based on dynamic equilibrium in the random walk of oxygen vacancies in the switching layer, experimentally observed as read noise. On long timescales, these statistics are remarkably stable, providing high data retention. However, the existing long-term degradation can be characterized by shifting and broadening of the programmed high resistive state distributions. A high endurance of more than 500 k cycles is demonstrated on the Mbit scale. Only a tail of a few devices appears to fail to reset. Via kinetic Monte Carlo modeling, the voltage divider of ReRAM cell and periphery has been identified as the origin of this failure.

1. Introduction

Redox-based resistive switching random access memory (ReRAM) has been extensively studied over the past years as promising nonvolatile memory (NVM) in the context of novel storage solutions. Recently, ReRAM is also considered as a key component in emerging neuromorphic computing systems. Here, ReRAM devices might resemble physical representations of artificial synapses.[1] Further, computation in memory concepts could be used to accelerate vector-matrix multiplications if the calculation is performed directly in the ReRAM array, significantly increasing the energy efficiency of the computation.[2]

Among other solutions, filamentary ReRAM based on the valence change mechanism (VCM) attracted a lot of attention. VCM devices, also referred to as OxRAM, typically consist of a metal oxide sandwiched between an active (AE) and an ohmic electrode (OE). Partial reduction of the oxide introduces oxygen vacancy states acting as mobile donors which can be rearranged during resistive switching operations and locally increase the electrical conductance. A comprehensive review of VCM was recently published by Dittmann et al.[3] The popularity of filamentary VCM can be explained by its outstanding characteristics being a cost-effective fabrication, high scalability, high switching speed,[4] and low power consumption.[3]

With respect to a large-scale industrial application of ReRAM, its reliability has to be characterized thoroughly and well understood, which requires tremendous statistics.[5] Apart from the market introduction, Strenz et al. identified three key challenges for emerging NVM,[6] being 1) read window at low ppm (i.e., low variability), 2) retention, and 3) endurance.

1) The read window between the high resistive state (HRS) and the low resistive state (LRS) is not only determined by the median HRS or LRS values, but also to a large extent by the variability within these states. The widths of the HRS and LRS distributions define down to which ppm level they can be distinguished, and thus provide the maximum number of devices in a memory block. As a consequence, it is highly relevant to investigate the different aspects of variability, to understand their physical origin, and to find ways of reducing the variability. 2) Once the statistics of HRS and LRS are understood, it has

S. Wiefels, R. Waser, S. Menzel
Peter-Grünberg-Institute 7 (PGI-7)
Forschungszentrum Jülich GmbH
52425 Jülich, Germany
E-mail: s.wiefels@fz-juelich.de

N. Kopperberg, D. Wouters, R. Waser
Institut für Werkstoffe der Elektrotechnik II (IWE II) and JARA-FIT
RWTH Aachen University
52074 Aachen, Germany

K. Hofmann, J. Otterstedt
Infineon Technologies AG
85579 Neubiberg, Germany

R. Waser
Peter-Grünberg-Institute 10 (PGI-10)
Forschungszentrum Jülich GmbH
52425 Jülich, Germany

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202300401.

DOI: 10.1002/pssa.202300401

to be investigated how stable these distributions are on long-time scales. To evaluate if they meet typical requirements like 10 years of retained information at an operating temperature of up to 85 °C, temperature-accelerated experiments have to be conducted. Here, reliable models to extrapolate the high-temperature retention down to the retention at operating temperature have to be provided. In terms of stability, not only long-term degradation has to be considered but also possible influences of the read operation on the programmed state called read disturb. 3) To assess the endurance of large memory blocks, comprehensive electrical measurements have to be performed. Here, the critical failure mechanisms affecting the weakest tail of the distribution need to be identified and understood to predict, avoid, or correct potential failures.

Lanza et al. recently reported on a gap in resistive switching research between academia and industry.[7] Embedded in a literature review, this article gives an overview of a joint project of RWTH Aachen and Infineon Technologies, which aims at closing this gap. We review the main findings reported from this cooperation and present the latest, new findings. Within this project, the key reliability aspects of variability (c.f. Section 2), retention (c.f. Section 3), read disturb (c.f. Section 4), and endurance (c.f. Section 5) have been addressed. We provide comprehensive electrical measurements, conducted on different generations of VCM, back end of line (BEOL) embedded in 28 nm CMOS technology. Although the different vehicles are not identical, they exhibit consistent, comparable characteristics. To support the experimental results, physical models were derived. To account for the intrinsic stochasticity in filamentary VCM ReRAM, the conducted simulations are based on kinetic Monte Carlo (KMC) models, ranging from 3D models with locally resolved activation energy for defect migration to compact 1D KMC solutions enabling the simulation of extensive endurance schemes.

2. Variability

As mentioned above, the stochasticity of the filamentary resistive switching operation is one of the key characteristics and challenges of VCM ReRAM.[8] This intrinsic variability can be observed in the switching voltages, SET/RESET times, and in the programmed states. These quantities can vary from device to device (D2D), from cycle to cycle (C2C), and the latter even from read to read (R2R).[3]

The D2D variability may be further distinguished into differences between devices on the same die, between dies, or even from wafer to wafer. One prominent aspect of D2D variability is the stochasticity of the forming process, manifesting in varying forming voltages.[9–11] For CMOS-integrated VCM, it has been shown that the D2D variability after forming can be achieved to be in the same order or lower than the C2C variability,[12,13] making it indistinguishable.

The C2C variability has been extensively studied in the context of endurance experiments (c.f. Section 5).[14] Here, the typical point clouds of device states (e.g., resistance) over cycle number reveal the state fluctuations from one cycle to the next. As the required voltage and time fluctuate as well,[15] switching errors may occur, which can be corrected by additional programming attempts with increased voltage or time. Thus, various programming algorithms have been developed to significantly reduce the C2C variability.[16–18]

2.1. R2R Variability - Read Noise or Short-Term Instability

However, the effect of programming algorithms is limited by the occurrence of an intrinsic R2R variability.[11,19,20] Observed as read noise or short-term instability, a programmed state is not entirely stable but exhibits characteristic fluctuations, as shown in **Figure 1**, for 20 k reads with constant voltage in a typical reading range.[21] Depicted are exemplary traces of devices in the HRS out of an experiment with 10 k devices of 28 nm BEOL VCM. Although the recorded states are overall quite stable, characteristic jumps between distinct levels occur randomly, which can cause bit errors during the programming algorithm as well as during read out.[21]

The same experimental data are used in the lag plot, as shown in Figure 1b, comparing the current of the first read out (#1) after programming to the one of the last read (#20 k). Although most of the 10 k devices are close to the diagonal line, meaning that their current did not change, several devices show fluctuations of more than 100% of their initial read current.

Characterizing whole memory blocks, it is hardly feasible to consider the characteristics of every single device. Instead, distributions of programmed states are evaluated. Figure 1c,d shows programmed HRS and LRS distributions of the same 10 k devices as cumulative distributions on a normalized probability scale (in normal percentiles). Whereas the LRS is plotted on a linear current scale, a logarithmic one was chosen for the HRS. As a result, the distributions in both states appear as straight lines, which identifies the LRS as normally distributed whereas the HRS follows a log-normal distribution. It was attempted to increase the read window by removing devices from the data set that exceeded a threshold. Instead of removing the data, those devices have been programmed by additional pulses into deeper HRS or LRS states. However, the distribution reverts back to its intrinsic (log-)normal shape. This reveals that the characteristic read noise plays a crucial role, as it generates a dynamic equilibrium characterized by the observed normal or log-normal statistics. These intrinsic statistics seem to be independent of the programming algorithm, and thus limit the achievable size of the read window.[19,21]

2.2. 3D KMC-Based Simulation Model

To improve the understanding of the intrinsic read noise, a 3D kinetic Monte Carlo (KMC) model was developed by Kopperberg et al.[22] This new model is based on the preliminary work of Abbaspour et al.[23] and was extended by the implementation of oxygen vacancy diffusion limiting domains. This extension was motivated by the work of Schie et al.[24] who found different diffusion regimes for oxygen vacancies in HfO_2 via molecular dynamics simulations. The key advantage of 3D KMC models over other simulation models is the ability to conduct statistical investigations of random processes. Furthermore, the extended model is able to explain several main aspects concerning variability and retention (cf. Section 3) by the same physical processes in one consistent model.

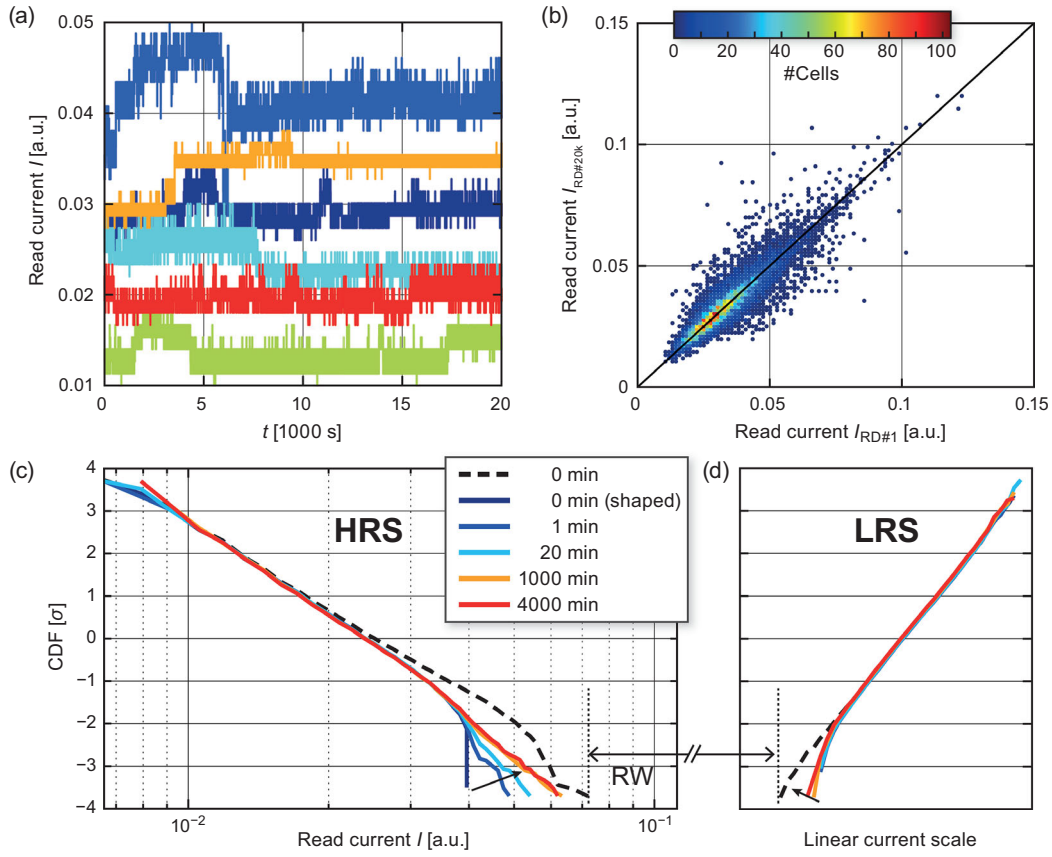

Figure 1. Read-to-read variability of embedded ReRAM. a) Characteristic read noise of exemplary devices over 20 000 reads. b) Galaxy plot comparing the read current of 10 k devices at the first read to the last read after 20 000 s. The color marks the number of devices at the respective data point. Most devices lie close to the black diagonal, representing no change between the two reads. However, current changes of up to 0.06 a.u. (>100%) are observed. c) HRS read current distributions containing 10 k devices in normal percentiles. The linear shape on the logarithmic current scale reveals log-normal statistics. From the initial distribution (dashed) devices with current above a threshold are removed from the data set. Subsequent reads relax back to the log-normal distribution. d) Corresponding LRS distributions following Gaussian statistics. Adapted from.[21]

As variability typically is much more present in the HRS than in the LRS,[19,25] Kopperberg et al. focused on this state in their simulations.[22] A typical HRS state, with oxygen vacancies (red) densely packed in the filament and lightly packed in the gap region above (both blue), is shown in **Figure 2**a. Here, the diffusion-limiting domains are represented by the cubic boxes throughout the whole device.

In Figure 2b, the current traces of three exemplary experimental (gray) ($Pt/ZrO_2/Ta$, see ref. [22] for more details) and three simulated (colored) VCM devices during a read pulse of 0.35 are presented. Due to the thermally activated random jumps of oxygen vacancies and the corresponding change in the read current, the simulations can nicely reproduce the experimental findings. Both current traces show discrete jumps of different heights, whereas the mean current of the traces stays rather constant. The only difference between the experiment and simulation is the high-frequent noise with low amplitude missing in the latter, as this electronic noise is not implemented in the model.[22] However, this is only a minor deviation, as the large current jumps related to ionic movement are much more critical concerning reliability. The zoom-in of the red simulated current trace in Figure 2c shows that the highest and most critical current jumps originated from oxygen vacancy jumps from the filament to the gap region or vice versa.[22]

As mentioned and shown in Figure 1c, the limited effectiveness of shaping algorithms is a key challenge concerning the variability of VCM. Thus, Kopperberg et al. moved from looking at individual devices to characterizing the statistics of many devices.[22] For the simulated devices in the HRS, the same log-normal distribution of the read current as in the experiment is observed. Furthermore, this distribution is in total very stable during typical read operation timescales. In Figure 2d, a simple shaping algorithm is applied by removing all devices above a certain current level, leading to the black curve with an enlarged read window. Here again, the random movement of oxygen vacancies can nicely explain the experimental observations, as the current distribution from our simulation reverts back to its initial shape.[22]

In summary, Kopperberg et al. were able to show that the random movement of oxygen vacancies is of major importance for the intrinsic log-normal behavior of the read current distribution in the HRS, the read noise of individual devices and the limitation of shaping algorithms.[22]

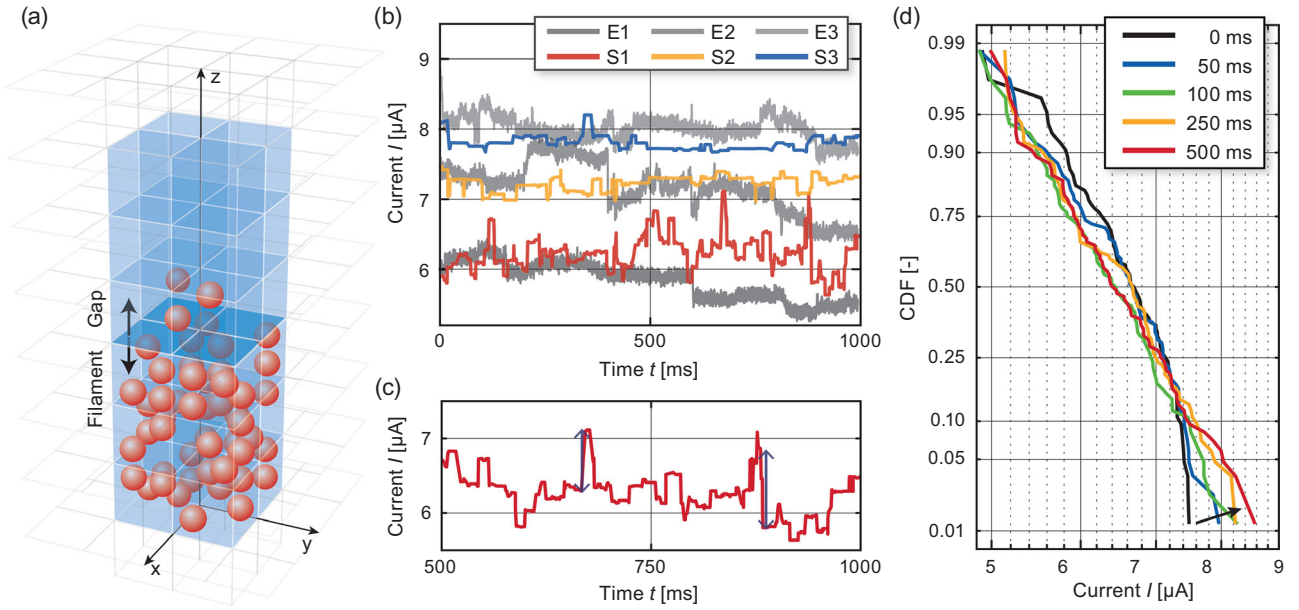

Figure 2. a) Sketch of a typical oxygen vacancy distribution in the HRS in the 3D KMC model with the newly introduced diffusion limiting domains. Here, the filament and gap region are highlighted in blue, with high defect (red balls) concentration in the filament and low defect concentration in the gap. Each cubic box corresponds to a diffusion-limiting domain. b) Current evolution over time during read pulse of exemplary experimental (gray) and simulated (colored) VCM devices programmed to the HRS. The experimental results are obtained on Pt/ZrO_2/Ta VCM devices with all details given in the study of Kopperberg et al.[22] c) Zoom in on the red curve (S1) from (b). The most critical jumps resulting in the highest current jumps marked by the blue arrows can be identified as oxygen vacancy jumps at the filament–gap interface. d) Current distribution of 100 simulated devices shows log-normal behavior. Initially ($t = 0$, black), all devices above a current limit of 7.5 are removed. Due to the movement of the oxygen vacancies, the distribution reverts back to its intrinsic log-normal behavior over time. Adapted under the terms of the CC-BY 4.0 license.[22] Copyright 2022, The Authors. Published by American Chemical Society.

3. Retention

The retention of a memory device describes the long-term stability of a programmed state. Typical requirements for NVM applications of ReRAM are 5–10 years at 85–125 °C.[3] Within this time at the respective storage temperature, the HRS or LRS has to be stable enough to ensure a sufficiently large read window. Several groups investigated the retention of VCM ReRAM: IMEC,[26] Panasonic,[27] Macronix,[28] MDM,[29] Politecnico di Milano,[30] Stanford University,[31] IHP Frankfurt,[32] LETI,[33] and Fudan University.[34] Most of the studies focus on the LRS and report decreasing read current.[26,27,30–34] The studies covering the HRS show mostly that the read current increases over time.[27–29] However also a decreasing HRS read current which is beneficial for the width of the read window is possible.[26]

An important aspect of retention studies is temperature-accelerated tests (also called accelerated life testing, ALT). As the retention target of several years is challenging to assess, the temperature is increased to shorten the timescales of the underlying degradation processes. The retention time (often mean time to failure, MTTF) is evaluated for different ($\geq$3) elevated temperatures and extrapolated according to Arrhenius' law down to the targeted operating temperature. This time is extracted as the point where the read current exceeds a certain threshold[32] or the resistance is changed by a defined factor.[33] However, it is challenging to extract the correct time constant for the physical process of degradation underlying the measured quantity, as discussed in the following section.

3.1. Experimental Retention

Wiefels et al. investigated the retention experimentally on 28 nm BEOL-integrated VCM.[35] On four dies, 2.5 M devices each were programmed into the HRS, stored at different elevated temperatures, and read out after increasing time intervals. The initial distributions for three exemplary dies are shown as blue lines in **Figure 3**.[35] It can be seen that most of each distribution follows log-normal statistics, whereas a tail close to the read window on the right side deviates from this shape. Upon annealing at the indicated temperatures ranging from 150 °C up to 260 °C, two effects are observed: 1) The distribution is shifted along the read current axis and 2) the distribution is tilted toward higher standard deviation σ, i.e., the distribution broadens.[35] This emphasizes that the long-term degradation of the HRS is much more complex than drifting or flipping toward the LRS. As explained above, retention evaluations often aim to determine an activation energy for the underlying degradation process. This is done by tracing the read current until a certain threshold is reached, marking the retention failure time, which is then added for different temperatures into an Arrhenius plot.[32,33] However, the observed statistical degradation raises the question of which percentile of the distribution the read current should be evaluated. Due to the rotation or broadening of the distribution over time, the speed of absolute resistance degradation increases with the evaluated percentile. Taking both observed processes (tilting and shifting) into account, one would even find that a current close to the median (0 σ) decreases whereas the current at −4 σ, close to the read window, increases.[21]

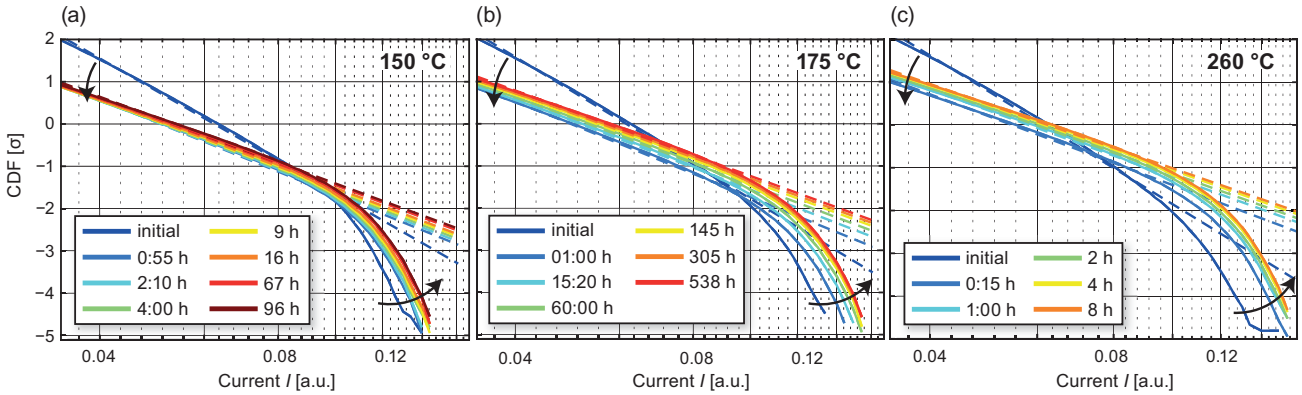

Figure 3. Read current distributions obtained by retention experiments at a) 150 °C, b) 175 °C, and c) 260 °C. All distributions show a tilt and shift during bake, whereas the general shape stays intact. Partially reproduced with permission.[35] Copyright 2020, IEEE.

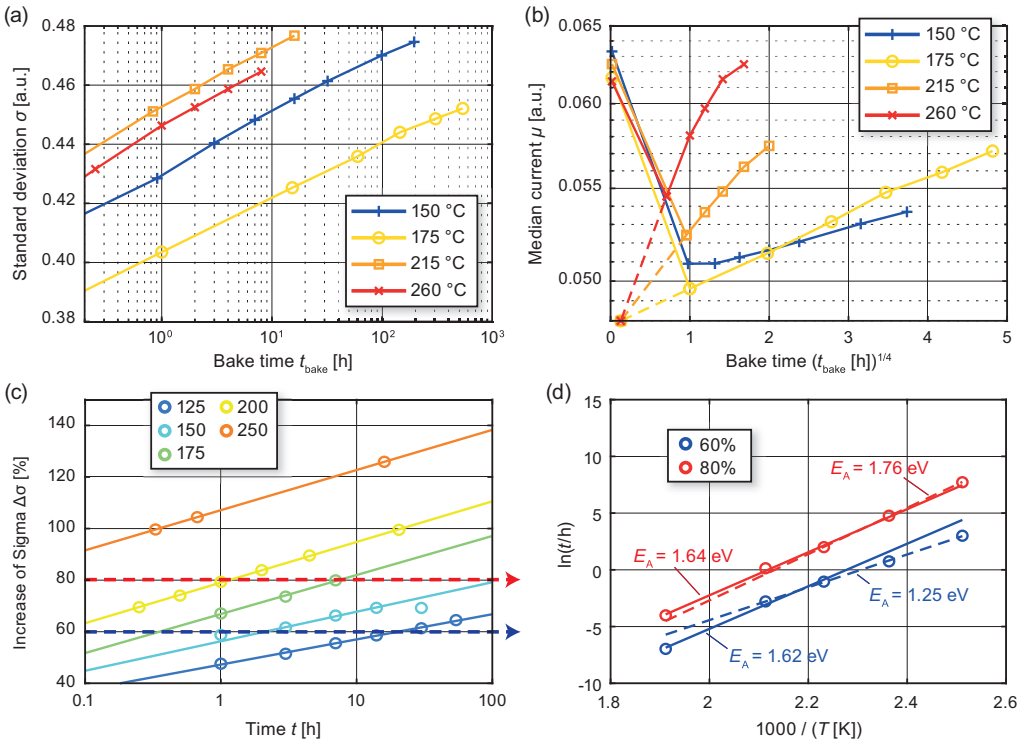

Figure 4. Characteristic parameters μ and σ of the log-normal distribution, extracted from linear fits in Figure 3. a) σ linearly increases with $\sigma \propto \log(t_{bake})$, b) μ initially decreases, subsequently increases linearly with $\mu \propto t^{1/4}$. c) Broadening of distribution over time to extract retention time for 60% and 80% increase in σ. d) Extracted retention times in Arrhenius plot to extract activation energy E_A. The fits with dashed lines favor low temperatures, whereas the solid lines are closer to the higher temperatures. Depending on fit and threshold, E_A results in a range from 1.25 eV to 1.76 eV. (a) and (b) Reproduced with permission.[35] Copyright 2020, IEEE. (c) and (d) Reproduced from.[21]

Thus, Wiefels et al. proposed to analyze the degradation based on the parameters of the underlying (log-normal) statistics.[21,36] For the data in Figure 3, this is done in **Figure 4**. Here, the log-normal distribution was fitted and its characteristic parameters μ and σ extracted. This gives a clear trend for the standard deviation σ in Figure 4a which linearly increases with the logarithmic annealing time $\log(t_{bake})$.[35] In contrast, the median μ in Figure 4b initially decreases until approx. 1 h and subsequently increases linearly with $(t_{bake})^{1/4}$. This indicates that two physical processes of degradation are competing, where the first is dominant until 1 h and superseded by the second. In combination, the degradation of the median μ appears as a minor issue for the retention. As a result, Wiefels et al. identified the continuous broadening of the distribution (c.f. Figure 4a) as the main aspect of long-term degradation.[35]

Further, it was demonstrated that the trend of the standard deviation σ can be used to derive an activation energy for the observed degradation.[21] To do this, Wiefels et al. repeated

the experiment on further samples covering five temperatures ranging from 125 °C to 250 °C, fitted the log-normal HRS distributions, and extracted the trend of σ.[21] Figure 4c shows its relative trend for the different temperatures. They defined two exemplary thresholds of degradation and transferred the time for 60% and 80% change of σ into the Arrhenius plot in Figure 4d. The resulting graphs are fitted linearly to extract the activation energy. Here, two different fits are applied, focusing either more on the high temperatures (solid lines) or the low temperatures (dashed lines). As a result, activation energies ranging from 1.25 eV up to 1.76 eV are found. Even here, the activation energy appears to depend on the defined thresholds. This extraction method, however, is much more consistent than the extraction via absolute changes in read current or resistance.[21]

Despite the availability of ALT schemes, the most solid approach to characterize retention is to monitor the degradation over long periods at operating temperatures if possible. For this study, we managed to read out over 36 M exemplary devices which were programmed 1376 days earlier (nearly 4 years). The resulting HRS and LRS distributions are shown in **Figure 5**.

The figure shows the initially programmed states in blue and the states after 1376 days of storage at room temperature in orange. After read out, all devices were rewritten using the original algorithm again. The resulting states are depicted by the red lines in Figure 5 which nearly perfectly coincide with the initial distributions, covering these optically. It is remarkable that the switching behavior did not change over this long time, and the devices can be reprogrammed perfectly. Apart from this, the degradation of the programmed states over nearly 4 years follows the general trends observed by our ALT strategy in Section 3. The median of the HRS distribution shifts toward a lower read current. The tilting (broadening) of the distribution leads to a shrinking read window, whereas the LRS distribution is very stable. Only a very slight decrease in read current may be detected. This underlines the validity of the ALT observations of our previous studies[21,35,36] and demonstrates that no additional, unexpected processes other than the ones accelerated during ALT occurred.

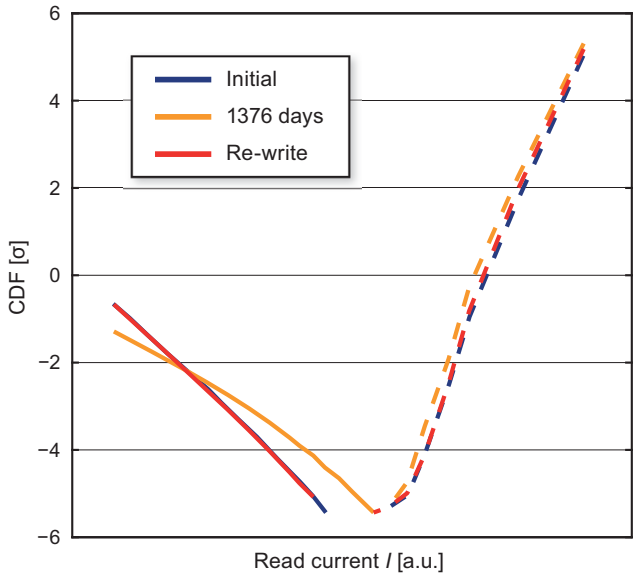

Figure 5. Retention of 36 M devices over 1376 days (nearly 4 years) at room temperature. The LRS is depicted by dashed lines, and the HRS by solid lines. The latter shows the predicted degradation after storage (orange), i.e., shifting of the median and broadening. The LRS distributions are very stable. After read out, all devices were reprogrammed with the original distributions leading to coinciding lines (initial blue distribution is covered by red reprogrammed data).

It may be noted that the dies for this experiment were not only stored at room temperature, but also transported via long-distance flights, cut, and packaged. Thus, we conclude that the devices not only show a high and predictable retention but also withstand the typical chip logistics.

3.2. 3D KMC-Based ALT Simulations

To expand the understanding of the physical processes underlying the long-term degradation of the VCM devices, Kopperberg et al. continued their work with the newly developed 3D KMC simulation model, as mentioned in Section 2.[22] By means of the same simulation model with the same physical assumptions used for the investigations of variability, they performed ALT simulations similar to the experiments. As before, they focused on the HRS.[22] A typical start configuration can be seen in **Figure 6**a, where the initial filament region with a high oxygen vacancy (red) concentration is marked by a blue box. To avoid confusion, the many smaller diffusion-limiting domains are not shown here anymore.

Performing the ALT simulations, where the VCMs have been exposed to high temperatures, two processes can be observed which are presented in (b) and (c) of Figure 6. On the one hand, the radial diffusion of oxygen vacancies away from the filament region is observed (Figure 6b). On the other hand, the vertical diffusion of oxygen vacancies from the filament to the gap region can be seen (Figure 6c).[22] In an average device, both processes take place overlain by each other at the same time, whereas in rare cases one of the processes dominates, leading to configurations, as shown in Figure 6b,c.[22]

As motivated before, it is much more informative to look at the statistics of multiple devices. Thus, Kopperberg et al. looked at the evolution of the current distribution of VCMs over time at an elevated temperature of 1000.[22] This comparatively high temperature is necessary in the simulations, as the computation time would otherwise be unacceptably long. The results of the simulations of VCM devices with two different initial HRS configurations are shown in **Figure 7** for a comparatively wide and in **Figure 8** for a comparatively narrow filament. In (a), the evolution of the current distribution can be seen, in (b) the mean current is depicted and in (c) the standard deviation change over time is presented. In all cases, the standard deviation of the current distributions increases over time, leading to a tilt of the distribution and thus a reduction of the read window. This process originates from the diffusion of oxygen vacancies away from a densely packed filament and seems to be most critical concerning the retention of VCM devices.[22] Depending on the initial state and the properties of the diffusion-limiting domains, the mean current of the distribution can either stay constant as in Figure 7, increase or decrease as in Figure 8. Here, it plays an important

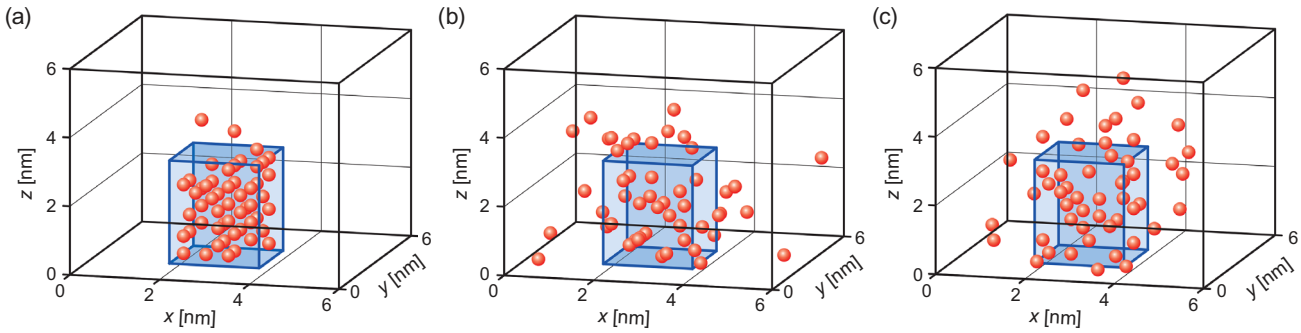

Figure 6. Sketches of exemplary oxygen vacancy (red balls) configurations in the oxide layer of a VCM device. The initial filament volume is represented by the blue box, for reasons of clarity, the many small diffusion-limiting boxes are not shown here. In a) A typical initial HRS configuration is shown, whereas b,c) show two exemplary final configurations after baking. In (b) the radial diffusion and in (c) the vertical diffusion into the gap region were dominant. Adapted under the terms of the CC-BY 4.0 license.[22] Copyright 2022, The Authors. Published by American Chemical Society.

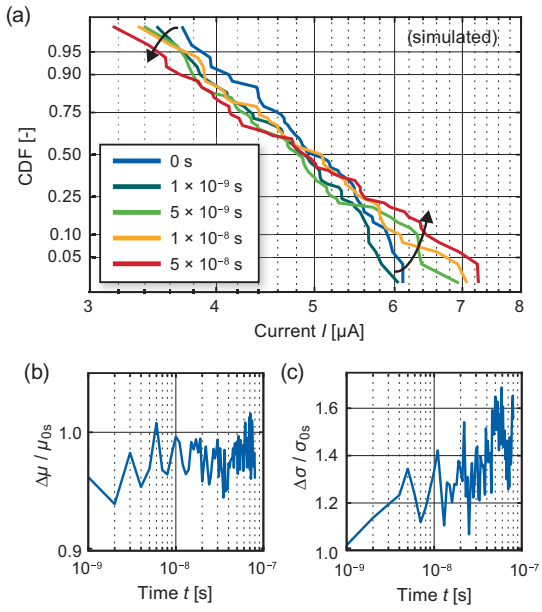

Figure 7. a) Evolution of the read current distribution during the baking simulation at 1000 for devices programmed to an HRS with comparatively wide filament. Here, b) the mean current stays roughly constant, whereas c) the standard deviation increases over time. Adapted under the terms of the CC-BY 4.0 license.[22] Copyright 2022, The Authors. Published by American Chemical Society.

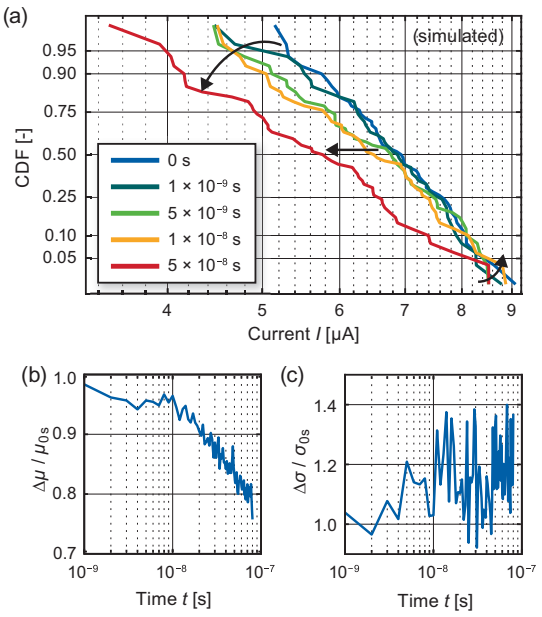

Figure 8. a) Evolution of the read current distribution during the baking simulation at 1000 for devices programmed to an HRS with comparatively narrow filament. Here, b) the mean current decreases, whereas c) the standard deviation increases during baking. Adapted under the terms of the CC-BY 4.0 license.[22] Copyright 2022, The Authors. Published by American Chemical Society.

role, whether the radial or the vertical oxygen vacancy diffusion is dominating. This also fits well to the experimental findings, where always a tilt of the distribution but depending on the study increasing or decreasing mean currents have been observed.[22]

4. Read Disturb

An important reliability aspect for nonvolatile memory is its stability against undesired influences of the read operation. It has to be clarified if the voltage stress of frequent read operations could potentially disturb the programmed states. For ReRAM, it has been demonstrated that the HRS can be affected by read pulses in SET polarity, typically investigated with comparatively high read voltages of $\geq$350 mV.[37,38] Here, it was shown that devices at a critical resistance state close to the read window are particularly vulnerable, whereas rather high resistive devices are stable even up to 700 mV.[37] Bengel et al. proposed to distinguish between all four combinations of resistance state (HRS/LRS) and reading polarity (SET/RESET).[39] Here, reading devices in HRS with SET polarity were identified as the most critical combination. However, disturb was only observed at elevated voltages $\geq$500 mV. Extrapolation down to 200 mV suggested a stable HRS at $-3\,\sigma$ (i.e., $\approx$1 kbit) for 10 years of continuous reading, which is more than sufficient.[39]

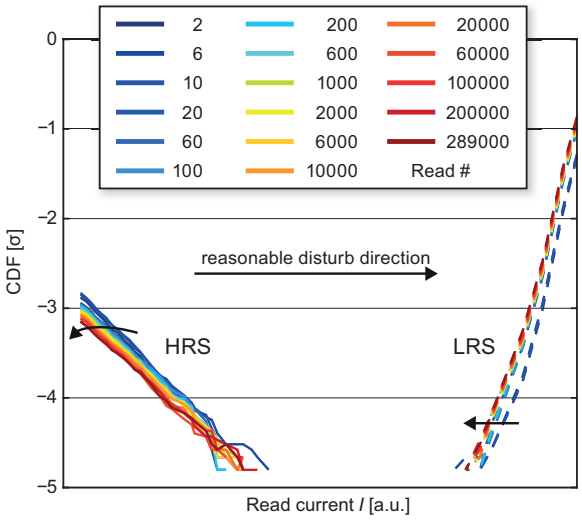

Figure 9. Reading stress test on HRS and LRS distributions of 1.3 M devices each. Both states are read repeatedly up to 289 000 times with a sense amplifier sweep with 52 steps, summing up to 15 M read pulses over 12 days. The resulting distributions are stable. The minor degradation cannot be attributed to read disturb, but rather to typical retention characteristics.

In this study, we investigated read disturb experimentally by repeatedly reading pre-programmed HRS and LRS distributions. **Figure 9** shows the results for 1.3 M ReRAM devices (28 nm BEOL VCM) per distribution read up to 289 000 times. After programming HRS and LRS by typical SET and RESET algorithms, both states were read by applying a typical read voltage (about one order of magnitude lower than the writing voltage) in SET direction. Here, each read is performed by a sense amplifier sweep, i.e., the read pulse is applied 52 times per read. In total, the data in Figure 9 account for 15 M read pulses. It can be stated that the programmed states are remarkably stable despite the high number of reads. Apart from small fluctuations at the tail due to read noise (c.f. Section 2), the visible effects on the distributions are a slight broadening as well as a small shift toward higher resistances. As the direction of this drift toward HRS contradicts the expected direction upon application of a (read) voltage in SET direction, it is unlikely to originate from read disturb. Nevertheless, both drifting and broadening can be explained as typical characteristics of the long-term degradation (c.f. Section 3). As the presented read operations were conducted over 12 days, it appears reasonable that the devices were not affected by reading at all, but rather show typical retention characteristics. Thus, read disturb appears to be no issue in these devices at a typical read voltage.

5. Endurance

Endurance denotes the maximum number of successful switching cycles (SET and RESET) a memory device can perform until permanent failure. Typical values reported for VCM ReRAM are 10^{7}[40] to 10^{10}[41,42] cycles. Some publications even demonstrate up to 10^{12} cycles.[43] However, these numbers are often demonstrated on single or few devices. They show either the upper end of feasibility for a given technology or the characteristics of typical devices. As discussed in the context of variability (Section 2) and retention (Section 3), the statistics over the whole memory block need to be taken into account. In the end, its performance is determined by the tail of weaker devices instead of the typical or best ones. A comprehensive overview of endurance characteristics along with guidelines for its characterization are given by Lanza et al.[14]

It has been demonstrated that endurance strongly depends on the applied biasing conditions.[44] If either of the writing processes is too strong, it can cause drifting of resistance states from cycle to cycle until it gets stuck in the respective state. Thus, it is crucial to balance the SET and RESET parameters.[44] We demonstrated in a previous study that this balancing can be performed by adaptive algorithms.[45] Via this algorithm, we determined the optimized endurance for different devices and revealed the influence of the ohmic electrode metal on the endurance. Here, a high barrier for the formation of additional oxygen vacancies at the interface of ohmic electrode and switching oxide was found to be beneficial. Otherwise, more and more defects are generated from cycle to cycle, leading to decreasing resistance until the device becomes stuck in LRS.[45] In conclusion, it is vital to optimize material combinations as well as programming conditions to ensure a high endurance reliability over many ReRAM devices.

5.1. Endurance of 2 Mbit BEOL-Integrated ReRAM

In a recent study, Kopperberg et al. investigated the endurance of 2 Mbit ReRAM BEOL integrated into 28 nm CMOS.[46] The block of 2 Mbit is part of a 16 Mbit test vehicle that is presented in **Figure 10**a and is highlighted in green. The devices are

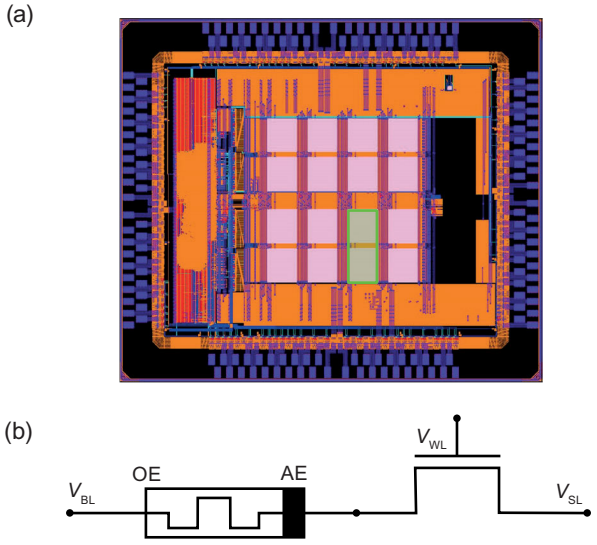

Figure 10. a) Image of the 16 Mbit testchip, with the block of 2 Mbit that was actually cycled in our experiments highlighted in green. b) Sketch of the 1T1R structure of the used VCM devices. The actual ReRAM element can be found on the left, the transistor on the right. VBL is connected to the Ohmic electrode (OE) of the ReRAM element, whereas the active electrode (AE) is connected to the transistor, leading to a $VBL > 0$ for the SET direction. Adapted under the terms of the CC-BY 4.0 license.[46] Copyright 2022, The Authors. Published by IEEE.

integrated in a typical 1-transistor-1-resistor (1T1R) configuration that is shown in Figure 10b.

The results of the experimental endurance study can be found in **Figure 11** as the cumulative HRS and LRS distributions are shown for different cycle numbers up to 500 k. SET and RESET as well as the initial forming process are performed with a program-verify algorithm, where the resistance of each bit is determined after each programming pulse and compared with a reference value. Until the reference value is reached, which is equivalent to a successful programming operation, it is repeated with, e.g., higher or longer pulses.[5]

In general, the investigated devices show great endurance as the LRS distribution only slightly broadens after 500 k cycles and the HRS distribution even drifts toward lower read currents leading to an increased read window. Nevertheless, from about 250 k cycles, a tail of bits that could not be RESET successfully appears in the HRS distribution. In the inset of Figure 11, it can be seen that this failure event only affects a few ppm of all devices, but due to the linearly increasing trend, this effect was studied further.[46] It may be noted that this is no end-of-life failure. All devices that were stuck at LRS could be recovered by additional RESET attempts.[46] To explain the observed RESET failure mechanism, Kopperberg et al. developed a simple phenomenological model where the resistances of a transistor and the other circuitry are summed up to a periphery resistance, that is in good approximation constant during the RESET operation.[46] This periphery and the cell resistance result in a voltage divider for the voltage that is actually dropping over the cell during RESET. They proposed that an unlucky combination of a high periphery and a low cell resistance leads to an insufficient cell voltage which causes the experimentally observed RESET failure.[46]

To support this theory, they developed a 1D KMC simulation model, which is based on the JART VCM 1.0 model by La Torre.[47] The main changes are the implementation of KMC methods to the central oxygen vacancy transition processes[48] and the addition of the periphery resistance, as can be seen in the equivalent circuit diagram in **Figure 12**. The central part of the model is located in the oxide layer, which is sandwiched between an ohmic and an active electrode. The oxide layer is divided into a low-ohmic plug region and a disc region with strongly varying resistance during the simulation, depending on the number of oxygen vacancies inside. This oxygen vacancy number is controlled by the exchange process between plug and disc, which is the main process of the simulation and is based on KMC methods and the Mott–Gurney law.[49] This model allows for the investigation of large statistics, which is necessary to investigate the influence of random and particularly rare processes.

In their simulations, Kopperberg et al. focused on the RESET operations. Thus, they considered typical values for the periphery resistances and initially programmed the devices to an LRS with a specific number of oxygen vacancies in the disc region, which mainly determines the device resistance. The read current distributions of the initial LRS can be found on the right side of **Figure 13**. Then, a typical RESET pulse is applied to the devices, resulting in the HRS distribution on the left side of Figure 13. To increase the probability of unlucky resistance combinations, the number of oxygen vacancies in the disc is increased (see color gradient), leading to more devices with critically low-ohmic

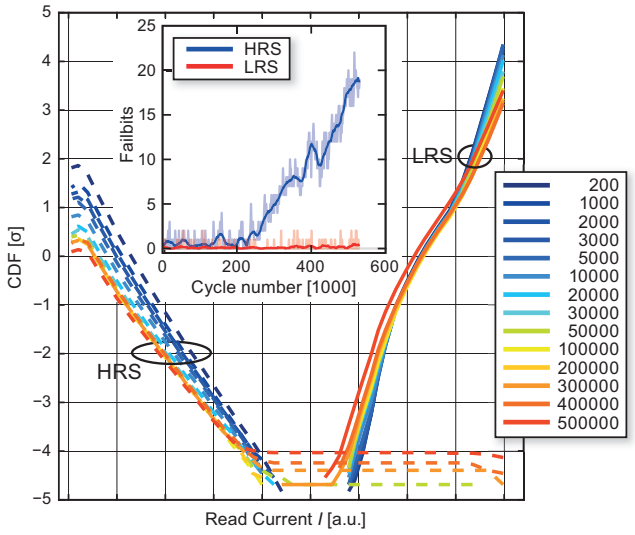

Figure 11. Distributions of HRS and LRS currents cycled up to 500 k times. In general, the devices show great endurance, but a rare RESET failure event can be observed after 500 k cycles for approx. 10 ppm of devices. The number of failed RESET (blue) and SET (red) operations per cycle, as well as a moving mean, are shown in the inset. The number of SET failure events stays constantly low, as the number of RESET failures increases linearly starting from approx. 250 k cycles. Adapted under the terms of the CC-BY 4.0 license.[46] Copyright 2022, The Authors. Published by IEEE.

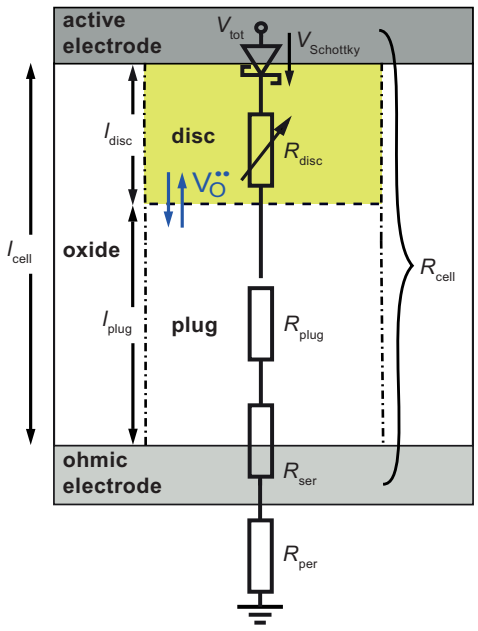

Figure 12. Equivalent circuit diagram of the 1D KMC model adapted with permission.[47] Oxygen vacancy exchange between plug and disc region was replaced by KMC methods and a periphery resistance was added. Adapted under the terms of the CC-BY 4.0 license.[46] Copyright 2022, The Authors. Published by IEEE.

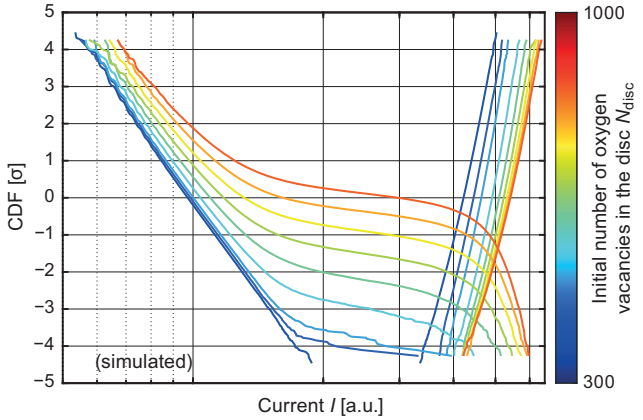

Figure 13. Simulated read current distributions of devices programmed to LRS (right) and after RESET (left). The color gradient indicates the number of oxygen vacancies in the disc for the initial LRS. Adapted under the terms of the CC-BY 4.0 license.[46] Copyright 2022, The Authors. Published by IEEE.

resistances. Resulting from that, more and more devices that are not completely (light blue and green) or not at all (orange and red) switched to the HRS can be observed. Additionally, the read currents of all devices before and after the RESET pulse are identified, showing that the higher the initial LRS current is, the more prone the device is to not switch to the HRS.[46] Even devices with higher read current after the RESET pulse than before have been identified.

Furthermore, Kopperberg et al. took a closer look at the properties of the devices, which got stuck in the LRS and did not switch to HRS during the RESET pulse.[46] In **Figure 14**, the failure probability of the devices is plotted in dependence on the periphery resistance and the initial number of oxygen vacancies in the disc, which directly corresponds to the device resistance. Finally, the initial prediction from the phenomenological model is underlined here, as in the simulations a combination of high periphery resistance and high number of oxygen vacancies in the disc (corresponding to a low device resistance) are required to observe the RESET failure.[46]

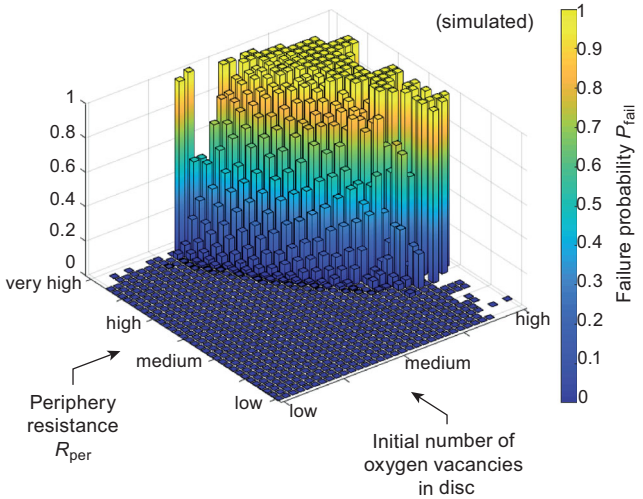

Figure 14. RESET failure probabilities of the devices in dependence on the periphery resistance and the initial number of oxygen vacancies in the disc. White panels indicate that no devices with these properties existed, whereas the color bar underlines the failure probability from dark blue (no failure) to yellow (all devices failed). Adapted under the terms of the CC-BY 4.0 license.[46] Copyright 2022, The Authors. Published by IEEE.

6. Conclusion

As summarized in this review, several reliability aspects have to be taken into account toward the commercial application of ReRAM in novel storage solutions. The key characteristic of filamentary VCM ReRAM is its inherent stochasticity. The resulting variability from D2D, C2C, and R2R has to be characterized and well understood. Whereas D2D and C2C can be minimized by fabrication and programming, an intrinsic read noise remains, which sets a limit to the minimum width of the read window. However, a well-understood limitation can be taken into consideration. Thus, successful programming in the range of Mbit was demonstrated. On long timescales, the degradation was found to affect the characteristic parameters of the read current distributions. The normal distribution in the LRS and the log-normal distribution in the HRS have been demonstrated to shift and broaden over time. We, therefore, recommend describing the retention by the stability of the underlying statistics. Using 3D KMC simulations, the random walk of oxygen vacancies was identified as the origin of both short-term instability and long-term degradation. Nevertheless, it has been demonstrated by temperature-accelerated measurements as well as by room temperature storage over 1376 days that the programmed states are exceptionally stable. Additionally, it was shown that the devices are not affected by read disturb.

Apart from the stability of the programmed states, the cycling endurance was thoroughly investigated. On 2 Mbit more than 500 k cycles have been demonstrated without any irreparable failures. A few devices that get temporarily stuck in LRS were identified as the most critical failure mechanism during cycling. Using compact 1D KMC simulations, these faults could be explained by the interplay of ReRAM device and access transistor, where unfavorable combinations of low device resistance and high transistor series resistance lead to insufficient voltage over the device. This increases the time required for switching and as a result, may lead to failed RESET attempts.

This demonstrates the high relevance of the access transistor for the memory device. It is therefore emphasized to focus future studies on understanding the complex interplay of ReRAM devices and transistors.

Acknowledgements

This work was supported in part by the Deutsche Forschungsgemeinschaft (SFB 917) and in part by the Federal Ministry of Education and Research (BMBF, Germany) in the project NEUROTEC (Project Nos. 16ME0398K and 16ME0399). It is based on the Jülich Aachen Research Alliance (JARA-FIT). The authors gratefully acknowledge computing time on the supercomputer JURECA at Forschungszentrum Jülich under grant no. 27525.

Open Access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

endurance, read disturb, reliability, retention, variabilities, valence change memories

Received: May 30, 2023
Revised: August 24, 2023
Published online: September 20, 2023

[1] D. Ielmini, Z. Wang, Y. Liu, *APL Mater.* **2021**, *9*, 050702.
[2] W. Wan, R. Kubendran, C. Schaefer, S. B. Eryilmaz, W. Zhang, D. Wu, S. Deiss, P. Raina, H. Qian, B. Gao, S. Joshi, H. Wu, H. P. Wong, G. Cauwenberghs, *Nature* **2022**, *608*, 504.
[3] R. Dittmann, S. Menzel, R. Waser, *Adv. Phys.* **2021**, *70*, 155.
[4] M. Csontos, Y. Horst, N. J. Olalla, U. Koch, I. Shorubalko, A. Halbritter, J. Leuthold, *Adv. Electron. Mater.* **2023**, *9*, 2201104.
[5] C. Peters, F. Adler, K. Hofmann, J. Otterstedt, in *2022 IEEE Int. Memory Workshop (IMW)*, IEEE, Piscataway, NJ **2022**, pp. 1–3.
[6] R. Strenz, in *Int. Memory Workshop*, Dresden, May 2020, pp. 1–4.
[7] M. Lanza, G. Molas, I. Naveh, *Nat. Electron.* **2023**, *6*, 260.
[8] P. K. Radtke, A. L. Hazel, A. V. Straube, L. Schimansky-Geier, *New J. Phys.* **2017**, *19*, 093007.
[9] A. Kindsmüller, A. Meledin, J. Mayer, R. Waser, D. J. Wouters, *Nanoscale* **2019**, *11*, 18201.
[10] C. Zambelli, A. Grossi, P. Olivo, D. Walczyk, T. Bertaud, B. Tillack, T. Schroeder, V. Stikanov, C. Walczyk, in *2014 Int. Conf. Microelectronic Test Structures (ICMTS)*, ICMTS Edinburgh, Scotland **2014**, pp. 27–31.
[11] A. Fantini, L. Goux, R. Degraeve, D. J. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y. Chen, B. Govoreanu, M. Jurczak, in *Int. Memory Workshop*, IEEE, Piscataway, NJ **2013**, pp. 30–33.
[12] A. Fantini, G. Gorine, R. Degraeve, L. Goux, C. Chen, A. Redolfi, S. Clima, A. Cabrini, G. Torelli, M. Jurczak, in *2015 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, Piscataway, NJ **2015**, pp. 7.5.1–7.5.4.
[13] C. Y. Chen, A. Fantini, L. Goux, G. Gorine, A. Redolfi, G. Groeseneken, M. Jurczak, *IEEE Electron Device Lett.* **2016**, *37*, 1112.
[14] M. Lanza, R. Waser, D. Ielmini, J. J. Yang, L. Goux, J. Suñe, A. J. Kenyon, A. Mehonic, S. Spiga, V. Rana, S. Wiefels, S. Menzel, I. Valov, M. A. Villena, E. , X. Jing, F. Campabadal, M. B. Gonzalez, F. Aguirre, F. Palumbo, K. Zhu, J. B. Roldan, F. M. Puglisi, L. Larcher, T. Hou, T. Prodromakis, Y. Yang, P. Huang, T. Wan, Y. Chai, et al., *ACS Nano* **2021**, *15*, 17214.
[15] F. Cüppers, S. Menzel, C. Bengel, A. Hardtdegen, M. von Witzleben, U. Böttger, R. Waser, S. Hoffmann-Eifert, *APL Mater.* **2019**, *7*, 091105/1.
[16] A. Glukhov, V. Milo, A. Baroni, N. Lepri, C. Zambelli, P. Olivo, E. Pérez, C. Wenger, D. Ielmini, in *2022 IEEE Int. Reliability Physics Symp. (IRPS)*, IEEE, Piscataway, NJ **2022**, pp. 3C.3–1–3C.3–7.
[17] E. R. Hsieh, X. Zheng, B. Q. Le, Y. C. Shih, R. M. Radway, M. Nelson, S. Mitra, S. Wong, *IEEE Electron Device Lett.* **2021**, *42*, 335.
[18] E. Perez, C. Zambelli, M. K. Mahadevaiah, P. Olivo, C. Wenger, *IEEE J. Electron Devices Soc.* **2019**, *7*, 740.
[19] S. Wiefels, C. Bengel, N. Kopperberg, K. Zhang, R. Waser, S. Menzel, *IEEE Trans. Electron Devices* **2020**, *67*, 4208.
[20] F. M. Puglisi, L. Larcher, A. Padovani, P. Pavan, *IEEE J. Emerging Sel. Top. Circuits Syst.* **2016**, *6*, 171.
[21] S. Wiefels, *Ph.D. Thesis*, Rheinisch-Westfaelische Technische Hochschule Aachen, **2021**.
[22] N. Kopperberg, S. Wiefels, S. Liberda, R. Waser, S. Menzel, *ACS Appl. Mater. Interfaces* **2021**, *13*, 58066.
[23] E. Abbaspour, S. Menzel, A. Hardtdegen, S. Hoffmann-Eifert, C. Jungemann, *IEEE Trans. Nanotechnol.* **2018**, *17*, 1181.
[24] M. Schie, M. P. Mueller, M. Salinga, R. Waser, R. A. D. Souza, *J. Chem. Phys.* **2017**, *146*, 94508/1.
[25] D. Ielmini, F. Nardi, C. Cagli, *Appl. Phys. Lett.* **2010**, *96*, 53503/1.
[26] Y. Y. Chen, R. Degraeve, S. Clima, B. Govoreanu, L. Goux, A. Fantini, in *2012 IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA **2012**, pp. 20.3.1–20.3.4.
[27] T. Ninomiya, S. Muraoka, Z. Wei, R. Yasuhara, K. Katayama, T. Takagi, *IEEE Electron Device Lett.* **2013**, *34*, 762.
[28] Y. Lin, Y. Ho, M. Lee, C. Wang, Y. Lin, F. Lee, K. Hsu, P. Tseng, D. Lee, K. Chiang, K. Wang, T. Tseng, C. Lu, in *IEDM*, IEEE, Piscataway, NJ **2017**, pp. 2.5.1–2.5.4.
[29] J. Frascaroli, F. G. Volpe, S. Brivio, S. Spiga, *Microelectron. Eng.* **2015**, *147*, 104.
[30] D. Ielmini, F. Nardi, C. Cagli, A. L. Lacaita, *IEEE Electron Device Lett.* **2010**, *31*, 353.
[31] S. Yu, Y. Y. Chen, X. Guan, H. Wong, J. A. Kittl, *Appl. Phys. Lett.* **2012**, *100*, 43507/1.
[32] E. Perez, M. K. Mahadevaiah, C. Zambelli, P. Olivo, C. Wenger, *J. Vac. Sci. Technol., B* **2019**, *37*, 012202.
[33] M. Azzaz, E. Vianello, B. Sklenard, P. Blaise, A. Roule, C. Sabbione, S. Bernasconi, C. Charpin, C. Cagli, E. Jalaguier, S. Jeannot, S. Denorme, P. Candelier, M. Yu, L. Nistor, C. Fenouillet-Beranger, L. Perniola, in *Int. Memory Workshop*, IEEE, Piscataway, NJ **2016**, pp. 1–4.
[34] Y. Wang, Y. Song, L. Yang, Y. Lin, R. Huang, Q. Zou, J. Wu, *IEEE Electron Device Lett.* **2012**, *33*, 1408.
[35] S. Wiefels, U. Böttger, S. Menzel, D. J. Wouters, R. Waser, in *2020 IEEE Int. Memory Workshop (IMW)*, Dresden, Germany, May 2020, pp. 28–31.
[36] S. Wiefels, U. Böttger, S. Menzel, D. J. Wouters, R. Waser, in *IEEE Int. Symp. VLSI Technology, Systems and Application (VLSI-TSA)*, IEEE, Piscataway, NJ **2020**, pp. 37–38.
[37] W. Shim, Y. Luo, J.-S. Seo, S. Yu, *IEEE Trans. Electron Devices* **2020**, *67*, 2318.
[38] T. Diokh, E. Le-Roux, S. Jeannot, P. Candelier, L. Perniola, J. Nodin, V. Jousseaume, T. Cabout, H. Grampei, E. Jalaguier, B. D. Salvo, in *IEEE Int. Integrated Reliability Workshop Final Report*, IEEE, Piscataway, NJ **2013**, http://dx.doi.org/10.1109/IIRW.2013.6804170.
[39] C. Bengel, J. Mohr, S. Wiefels, A. Singh, A. Gebregiorgis, R. Bishnoi, S. Hamdioui, R. Waser, D. Wouters, S. Menzel, *Neuromorph. Comput. Eng.* **2022**, *2*, 034001.
[40] G. Sassine, D. A. Robayo, C. Nail, J.-F. Nodin, J. Coignus, G. Molas, E. Nowak, in *2018 IEEE Int. Memory Workshop (IMW)*, IEEE, Piscataway, NJ **2018**, pp. 1–4.
[41] H. Lee, Y. Chen, P. Chen, P. Gu, Y. Hsu, S. Wang, W. Liu, C. Tsai, S. Sheu, P. Chiang, W. Lin, C. Lin, W. Chen, F. Chen, C. Lien, M. Tsai, in *Technical Digest - Int. Electron Devices Meeting, IEDM*, IEDM, San Francisco, CA, USA **2010**, pp. 19.7.1–19.7.4.
[42] X. D. Huang, Y. Li, H. Y. Li, K. H. Xue, X. Wang, X. S. Miao, *IEEE Electron Device Lett.* **2020**, *41*, 549.
[43] Y.-B. Kim, S. R. Lee, D. Lee, C. B. Lee, M. Chang, J. H. Hur, M.-J. Lee, G.-S. Park, C. J. Kim, U.-I. Chung, I.-K. Yoo, K. Kim, in *IEEE Symp. VLSI Technology (VLSIT)*, IEEE, Piscataway, NJ **2011**, p. 52.

[44] Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. Kar, D. Wouters, G. Groeseneken, J. Kittl, M. Jurczak, L. Altimime, *IEEE Trans. Electron Devices* **2012**, *59*, 3243.
[45] S. Wiefels, M. von Witzleben, M. Hüttemann, U. Böttger, R. Waser, S. Menzel, *IEEE Trans. Electron Devices* **2021**, *68*, 1024.
[46] N. Kopperberg, S. Wiefels, K. Hofmann, J. Otterstedt, D. J. Wouters, R. Waser, S. Menzel, *IEEE Access* **2022**, *10*, 122696.
[47] C. L. Torre, A. F. Zurhelle, S. Menzel, in *2019 Int. Conf. Simulation of Semiconductor Processes and Devices (SISPAD)*, SISPAD, Yokohama, Japan **2019**, pp. 1–4.
[48] S. Menzel, B. Wolf, S. Tappertzhofen, I. Valov, U. Böttger, R. Waser, in *2014 6th IEEE Int. Memory Workshop (IMW)*, Taipeh, Taiwan **2014**, pp. 42–45.
[49] N. F. Mott, R. W. Gurney, *Electronic Processes in Ionic Crystals*, 2nd ed., Oxford at the Clarendon Press, Oxford, UK **1950**.

Stefan Wiefels was born in Grevenbroich, Germany. He received his M.Sc. degree in materials science and Ph.D. degree in electrical engineering and information technology from RWTH Aachen University, Aachen, Germany, in 2016 and 2021, respectively. His current research focuses on the electrical characterization of memristive devices with respect to variability, reliability, and their application in neuromorphic circuits.

Nils Kopperberg was born in Gummersbach, Germany. He received his B.Sc. and M.Sc. degree in physics with a focus on nanoelectronics from RWTH Aachen University, Aachen, Germany, in 2016 and 2019, respectively. There, he is currently pursuing Ph.D. degree in electrical engineering, focusing on the physical modeling and the simulation of ReRAM. Mainly the reliability, statistical effects, and failure mechanisms are in the scope of his work.

Karl Hofmann was born in Mannheim, Germany. He has studied physics and received his PhD from RWTH Aachen in 2001. Karl joined Infineon Technologies as a development engineer and published several articles on device reliability. Currently, he is focusing on the development of emerging nonvolatile memories and is a member of the technical committee of the International Memory Workshop (IMW).

Jan Otterstedt was born in Bremen, Germany. He studied electrical engineering at the University of Hannover, Germany, and in 1997 received his Dr.-Ing. degree. Afterward, Jan joined the semiconductor group of Siemens, which later became the Infineon Technologies AG. For more than 15 years, he has been responsible for concept engineering for embedded nonvolatile memories. Since 2006, Jan also lectures on "Testing Digital Circuits" at the Technische Universität München (TUM).

Dirk J. Wouters received his master's and Ph.D. degrees in electrical engineering from the University of Leuven, Leuven, Belgium, in 1982 and 1989, respectively. In 2014, he joined the Institute of Electronic Materials, RWTH Aachen University, Aachen, Germany, where he focused on the research of metal-oxide-based RRAM.

Rainer Waser received his Ph.D. degree in physical chemistry from the University of Darmstadt, Darmstadt, Germany, in 1984. In 1992, he joined the Faculty of Electrical Engineering and Information Technology, RWTH Aachen University, Aachen, Germany as a professor and in 2007 as a director of the Institute of Solid State Research, Forschungszentrum Jülich, Jülich, Germany, in 1997. He was a recipient of the prestigious Gottfried Wilhelm Leibniz Preis in 2014.

Stephan Menzel was born in Bremen, Germany. He received the diploma degree and the Ph.D. degree (*summa cum laude*) in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2005 and 2012, respectively. He is currently a senior researcher with the Peter-Grünberg-Insitut 7, Forschungszentrum Jülich GmbH, Jülich, Germany, where he is also leading the Simulation Group.